_	86	<pre>capacitor.ti. and(second near polarity)) and(first near polarity</pre>	USPAT; US-PGPUB;	2004/10/18 13:28
-	73	((capacitor.ti. and(second near polarity)) and(first near polarity)) and(terminal\$1)	JPO USPAT; US-PGPUB;	2004/10/18 13:29
_	57	polarity)) and(first near polarity))	JPO USPAT; US-PGPUB;	2004/10/18 13:29
-	1	<pre>polarity)) and(first near polarity)) and(terminal\$1)) and(electrode or plate))</pre>	JPO USPAT; US-PGPUB; JPO	2004/10/18 13:29
_	27	<pre>and(anode) ((((capacitor.ti. and(second near polarity)) and(first near polarity)) and(terminal\$1)) and(electrode or plate))</pre>	USPAT; US-PGPUB; JPO	2004/10/18 13:29
-	23	and(anode or positive)	USPAT; US-PGPUB; JPO	2004/10/18 14:47
-	9	capacitor near package.ti. and(terminal\$1)	USPAT; US-PGPUB; JPO	2004/10/18 14:49
-	22	capacitor.ti. and(second near polarity near terminal\$1)	USPAT; US-PGPUB; JPO	2004/10/19 08:57
-	415	storage with capacitor.ti.	USPAT; US-PGPUB; JPO	2004/10/19 08:57
-	29	361/\$.ccls. and storage with capacitor.ti.	USPAT; US-PGPUB; JPO	2004/10/19 09:25
_	0	MLc with capacitor.ti. and(anode)	USPAT; US-PGPUB; JPO	2004/10/19 09:25
_	15	multilayer with capacitor.ti. and(anode)	USPAT; US-PGPUB; JPO	2004/10/19 09:26
-	13	<pre>multilayer with capacitor.ti. and(anode)) and(cathode</pre>	USPAT; US-PGPUB; JPO	2004/10/19 09:36
_	0	capacitor near package and(fan with plate)	USPAT; US-PGPUB; JPO	2004/10/19 09:36
_	15565	fan with plate	USPAT; US-PGPUB; JPO	2004/10/19 09:36
_	741203	electrode wit fan with plate	USPAT; US-PGPUB; JPO	2004/10/19 09:36
-	1680086	h	USPAT; US-PGPUB; JPO	2004/10/19 09:36
-	105	electrode with fan with plate	USPAT; US-PGPUB; JPO	2004/10/19 09:42
-	37	capacitor.ti. and(plate near assembly)	USPAT; US-PGPUB; JPO	2004/10/19 09:43
-	1	multi adj layer with capacitor.ti. and(second near plate)	USPAT; US-PGPUB; JPO	2004/10/19 09:45
-	0	multi adj layer with capacitor.ti. and(rectangular near volume)	USPAT; US-PGPUB; JPO	2004/10/19 09:45
_	24	multi adj layer with capacitor.ti. and(rectangular)	USPAT; US-PGPUB; JPO	2004/10/19 09:53

-	0	multi adj layer with capacitor.ti. and(anode)	USPAT; US-PGPUB;	2004/10/19 09:53
-	2	multi adj layer with capacitor.ti. and(positive near electrode)	JPO USPAT; US-PGPUB; JPO	2004/10/20 07:29
-	49	capacitor.ti. and(terminal\$1 with first near polarity)	USPAT; US-PGPUB; JPO	2004/10/20 07:29
-	34	capacitor.ti. and(terminal\$1 with first near polarity)) and(terminal\$1 with second near polarity	USPAT; US-PGPUB; JPO	2004/10/20 08:38
-	16	1	USPAT; US-PGPUB; JPO	2004/10/20 08:12
-	0	<pre>(((capacitor.ti. and(terminal\$1 with first near polarity)) and(terminal\$1 with second near polarity)) and(motherboard))</pre>	USPAT; US-PGPUB; JPO	2004/10/20 08:38
-	1	<pre>and(voltage near regulat\$3) ((capacitor.ti. and(terminal\$1 with first near polarity)) and(terminal\$1 with second near polarity)) and(motherboard)</pre>	USPAT; US-PGPUB; JPO	2004/10/20 08:40
_	1	<pre>(((capacitor.ti. and(terminal\$1 with first near polarity)) and(terminal\$1 with second near polarity)) and(motherboard)) and(chip)</pre>	USPAT; US-PGPUB; JPO	2004/10/20 08:40
-	0	<pre>(((((capacitor.ti. and(terminal\$1 with first near polarity)) and(terminal\$1 with second near polarity)) and(motherboard)) and(chip)) and(memory)) and(voltage)</pre>	USPAT; US-PGPUB; JPO	2004/10/20 08:41
-	1	<pre>(((((capacitor.ti. and(terminal\$1 with first near polarity)) and(terminal\$1 with second near polarity)) and(motherboard))</pre>	USPAT; US-PGPUB; JPO	2004/10/20 08:45
-	74338	<pre>and(chip)) and(memory)) and(power) system.ti. and(regulat\$3)</pre>	USPAT; US-PGPUB; JPO	2004/10/20 08:45
-	560	system.ti. and(regulat\$3)) and(motherboard	USPAT; US-PGPUB; JPO	2004/10/20 08:45
-	309	<pre>((system.ti. and(regulat\$3)) and(motherboard)) and(chip)</pre>	USPAT; US-PGPUB; JPO	2004/10/20 08:45
-	281	<pre>(((system.ti. and(regulat\$3)) and(motherboard)) and(chip)) and(memory)</pre>	USPAT; US-PGPUB; JPO	2004/10/20 08:45
_	257	<pre>(((((system.ti. and(regulat\$3)) and(motherboard)) and(chip)) and(memory)) and(bus)</pre>	USPAT; US-PGPUB; JPO	2004/10/20 08:46
-	15	<pre>((((((system.ti. and(regulat\$3)) and(motherboard)) and(chip)) and(memory)) and(bus)) and(synchronous near dynamic)</pre>	USPAT; US-PGPUB; JPO	2004/10/20 08:49
-	8	<pre>(((((((system.ti. and(regulat\$3)) and(motherboard)) and(chip)) and(memory)) and(bus)) and(synchronous near dynamic)) and(capacitor)</pre>	USPAT; US-PGPUB; JPO	2004/10/20 08:47
_	0	<pre>(((((capacitor.ti. and(terminal\$1 with first near polarity)) and(terminal\$1 with second near polarity)) and(motherboard))</pre>	USPAT; US-PGPUB; JPO	2004/10/20 08:49
-	75	and(chip)) and(memory)) and(bus) system.ti. and(regulat\$3)) and(memory with synchronous near dynamic	USPAT; US-PGPUB; JPO	2004/10/20 08:50
_	0	((system.ti. and(regulat\$3)) and(memory with synchronous near dynamic)) and(dynamic near randon near access near	USPAT; US-PGPUB; JPO	2004/10/20 08:51
-	66	memory) ((system.ti. and(regulat\$3)) and(memory with synchronous near dynamic)) and(dynamic near random near access near	USPAT; US-PGPUB; JPO	2004/10/20 08:51
	L	memory)		